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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/887,925	06/22/2001	Aniruddha P. Joshi	42390.P11393	7464

7590 03/18/2005

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EXAMINER	
VU, TRISHA U	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 03/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/887,925	JOSHI ET AL.	
	Examiner	Art Unit	
	Trisha U. Vu	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 8, and 9 rejected under 35 U.S.C. 102(e) as being anticipated by Miner et al. (6,690,655) (hereinafter Miner).

As to claim 1, Miner teaches a computer peripheral device (RIU 209 or RIU 210) comprising: a memory for storing a configuration address (obtaining an address configuration) (col. 11, lines 42-67); and an independent power level control circuit (processor 409 and associate circuitry) for controlling the power level in the device so as to be in a standby mode (standby mode) or normal power mode (power up/active mode) after power is applied to the device (col. 12, lines 1-17), the circuit being coupled to the memory to control an initial assignment of configuration address from a bus to the memory (e.g. bus 213) when the circuit enters a normal power mode after it is activated by a software application (upon powered up) (Fig. 4 and col. 5 lines 58-67, col. 11 lines 42-67).

As to claim 8, Miner teaches a computer system comprising: a processor (network control facility 205); and a plurality of peripheral devices (RIUs 209, 210) coupled to the processor through at least one bus (e.g. bus 213) (Fig. 2), each device having a power level control circuit (processor 409 and associate circuitry) for causing the device to be in a standby mode (standby mode) or normal power mode (power up/active mode) once power is applied to the device (col. 12, lines 1-17) and storage circuit for storing a configuration address (obtaining an address configuration) (col. 11, lines 42-67), the storage circuit storing a configuration address from the bus when the power level control circuit initially causes the device to be in the normal operating mode (Fig. 4 and col. 11, lines 42-67).

As to claim 9, Miner further teaches the bus is an address bus (the bus delivers address information to the RIU) (at least col. 9, lines 28-49 and col. 11, lines 42-67).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2-5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miner et al. (6,690,655) (hereinafter Miner) in view of Michael (5,787,306).

As to claims 2-3, the argument above for claim 1 applies. However, Miner does not explicitly disclose once storing a configuration address, retaining that address until the device is reset or power is turned on or off, and the memory device does not change its stored address when the device is reconfigured. Michael teaches once storing a configuration address, retaining that address until the device is reset or power is turned on or off, and the memory device does not change its stored address when the device is reconfigured (retaining the address of the device and configuring the address again each time the system is powered up) (col. 6, lines 35-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include once storing a configuration address, retaining that address until the device is reset or power is turned on or off, and the memory device does not change its stored address when the device is reconfigured as taught by Michael in the system of Miner to save time for address configuration process since the address is retained until the system is powered up again.

As to claim 4, Miner further teaches the bus is an address bus (the bus delivers address information to the RIU) (at least col. 9, lines 28-49 and col. 11, lines 42-67).

As to claim 5, Michael further teaches restoring an address after a reset signal is received by the circuit or power is turned on or off (Fig. 4, and col. 6, lines 35-40).

As to claim 7, the argument above for claim 1 applies. However, Miner does not explicitly disclose restoring an address after a reset signal is received by the circuit or power is turned on or off. Michael teaches the memory restores an address after a reset signal is received by the circuit or power is turned on or off (retaining the address of the device and configuring the address again each time the system is powered up) (col. 6, lines 35-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to restore an address after a reset signal is received by the circuit or power is turned on or off as taught by Michael in the system of Miner to save time for address configuration process since the address is retained until the system is powered up again.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miner et al. (6,690,655) (hereinafter Miner) in view of Michael (5,787,306) as applied to claim 5 above, and further in view of Applicant's Admitted Prior Art (hereinafter AAPA).

As to claim 6, Miner and Michael not explicitly disclose the circuit is responsive to two addresses once a configuration address is stored. AAPA teaches peripheral devices which are responsive to two addresses (two addresses are required for operation of the peripheral device in most instances

such as for SIO) (page 2, paragraph [0004] and page 6, paragraph [0013]). It would have been obvious to one of ordinary skill in the art to include peripheral devices responsive to two addresses as taught by AAPA in the system of Michael to allow operation of peripheral devices such as SIO.

5. Claims 10-11 and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miner et al. (6,690,655) (hereinafter Miner) in view of Amin et al. (6,429,706) (hereinafter Amin).

As to claim 10, the argument above for claim 8 applies. However, Miner does not explicitly disclose each of the peripheral devices is initially sequentially brought into a normal operating mode. Amin teaches each of the peripheral devices is initially sequentially brought into a normal operating mode (sequentially power up each device) (col. 1, lines 34-41 and 58-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement sequentially bring each of the peripheral devices into a normal operating as taught by Amin in the system of Miner to avoid potentially damaging power spikes (col. 1, lines 34-41).

As to claim 11, Amin further teaches the peripheral devices are sequentially powered up after a reset or after power is turned on or off (col. 3, lines 40-45).

As to claim 16, Miner teaches a method for operating a computer system comprising: applying power to a plurality of peripheral devices; entering a power

standby mode in the plurality of peripheral devices storing a unique configuration address in each device as the device enters the normal mode (upon powered up) (Figs. 2, 4, and col. 11 line 42 to col. 12 line 17). However, Miner does not explicitly disclose sequentially entering a normal mode from a standby mode for each peripheral device. Amin teaches sequentially entering a normal mode for each peripheral device (col. 1, lines 34-41). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement sequentially entering a normal mode for each peripheral device as taught by Amin in the system of Miner to avoid potentially damaging power spikes (col. 1, lines 34-41).

As to claim 17, Miner further teaches the storing step occurs after reset (powered up) (col. 11, lines 42-67).

As to claim 18, Miner further teaches the storing step for each peripheral device includes the reading of data from a bus (obtaining an address configuration) (col. 11, lines 42-67).

As to claim 19, Miner I further teaches the reading of data from a bus comprises the reading of data from a data bus and an address from an address bus (obtaining address configuration, software updates,... via address/data bus 213) (col. 11, lines 42-67).

As to claim 20, Miner further teaches configuring each peripheral device after it has stored its configuration address (e.g. obtaining physical layer communications configuration) (col. 11, lines 42-67).

6. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miner et al. (6,690,655) (hereinafter Miner) in view of Henrikson (6,163,823).

As to claim 12, Miner teaches a computer system comprising: a processor (network control facility 205); an output unit (207) coupled to the processor; and a plurality of peripheral devices (RIUs 209, 210) each being coupled to a bus (e.g. buses 212, 213) and each being coupled to a power level control line (e.g. via bus 213) from the output unit, signals over the control line causing each device to be placed in a standby mode or normal operating mode after power is applied to the device (Figs. 2, 4, and col. 11 line 42 to col. 12 line 17), each peripheral device having a memory which receives and stores a configuration address from the bus in response to a signal on the power level control line (upon powered up) which causes the device to enter a normal operating mode (col. 11 line 42 to col. 12 line 17). However, Miner does not explicitly disclose each peripheral device has a separate respective control line. Amin teaches separate control line (keyline) to enable each device (abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement separate control line for each device as taught by Henrikson in the system of Amin to allow fast access to the devices (col. 1, lines 34-41).

As to claim 13, Miner further teaches the bus is coupled between the output unit and the peripheral devices (Fig. 2).

As to claim 14, Miner further teaches the bus is an address bus (the bus delivers address information to the RIU) (at least col. 9, lines 28-49 and col. 11, lines 42-67).

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miner et al. (6,690,655) (hereinafter Miner) in view of Henrikson (6,163,823) as applied to claim 12 above, and further in view of Michael (5,787,306).

As to claim 15, Miner does not explicitly disclose the memory of each of the peripheral devices store a configuration address only when first entering the normal operating mode after a reset or after power is turned on or off. Michael teaches storing a configuration address only when first entering the normal operating mode after a reset or after power is turned on or off (retaining the address of the device and configuring the address again each time the system is powered up) (col. 6, lines 35-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to store a configuration address only when first entering the normal operating mode after a reset or after power is turned on or off as taught by Michael in the system of Miner and Henrikson to save time for address configuration process since the address is retained until the system is powered up again.

Response to Arguments

1. Applicant's arguments filed on 12/20/2004 have been fully considered but they are not persuasive.

2. In response to the applicant's arguments that Miner fails to disclose the assignment of configuration address from the bus to the memory is under control of the power level control circuit, which only enters into the normal power mode when activated by the software application. Miner anticipates these limitations as cited in col. 11, lines 42-67. Miner teaches the RIUs 209, 210 connecting to the network control facility 205 via the buses 212, 213 and 215 as shown in figure 2. Miner teaches the RIUs 209, 210 comprise three process states: 1) a boot-up state, 2) a standby state, 3) active mode processing state. Wherein, state 1) a boot-up state comprising the step of self-diagnostic tests, and registers with the network control facility 205 via the buses 212, 215. During the boot-up state the RIUs 209, 210 receive configuration parameters, which include address configuration from the network control facility 205 via buses 212-213, 215. The address configuration is stored in the network control facility 205 and it is being transferred to the RIUs 209, 210 during the boot-up state via the buses 212-213, 215. Therefore, there is a memory for storing the address configuration in the network control facility 205 and it is connecting to the buses 212-213, 215 in order to transfer configuration parameters to the RIUs 209, 210. Further, RIUs 209, 210 comprising active mode processor 407 and standby mode processor 409 for power conservation after the RIUs is boot-up by the boot-up process. Column 12 lines 1-17, Miner teaches the RIU 209, 210 comprising the standby mode and active mode after they completed their boot-up processing. Column 12 lines 10-17, Miner teaches the processor 409 powers up the active mode (normal processing) processor 407 if there is an interrupt requesting for service.

3. In the office action, Examiner clearly reasoning why Michael (5,787,306), Amin et al. (6,429,706), Henrikson (6,163,823) are combined to Miner because these references teach limitations lack from Miner and they all suggested to combine the lack limitations in order to improve the Miner's system. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made combine these references.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha U. Vu whose telephone number is 703-305-5959. The examiner can normally be reached on Mon-Thur and alternate Fri from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trisha U. Vu
Examiner
Art Unit 2112

TIM VO
PRIMARY EXAMINER